

P-Channel 60-V(D-S) Enhancement Mode Field Effect Transistor

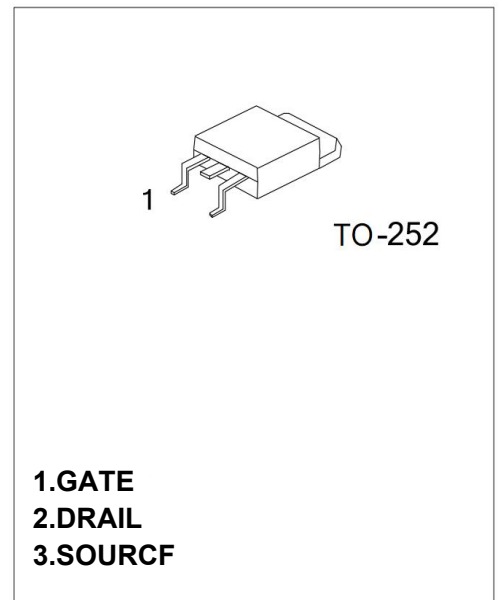
V(BR)DSS	RDS(on)MAX	ID
-60 V	200mΩ@ -10 V	-8.8A

General Description:

Third generation Power MOSFETs from Vishay provide the designer with the best combination of fast switching, ruggedized device design, low on-resistance and cost-effectiveness.

The is designed for surface mounting using vapor phase, infrared, or wave soldering techniques. The straight lead version (IRFRseries) is for through-hole mounting applications. Power dissipation levels up to 1.5 W are possible in typical surface mount applications.

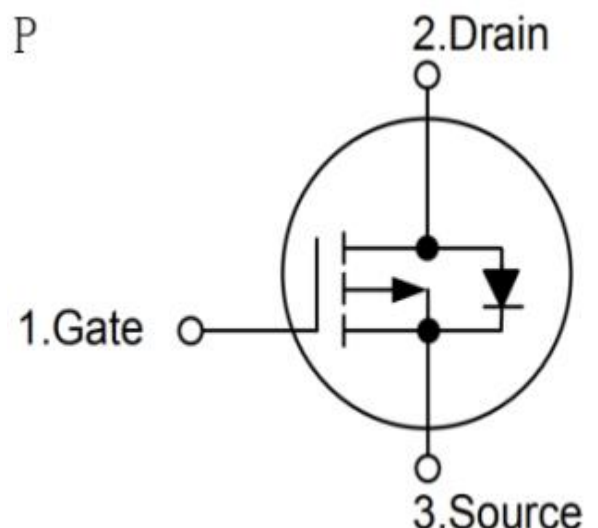
Equivalent Circuit:



FEATURE:

- ※ Surface Mount
- ※ Straight Lead
- ※ Available in Tape and Reel
- ※ Fast Switching
- ※ Repetitive Avalanche Rated
- ※ Simple Drive Requirements
- ※ Lead (Pb)-free Available.
- ※ Dynamic dV/dt Rating
- ※ Ultra Low On-Resistance

SYMBOL :



Maximum ratings (Ta=25°C unless otherwise noted)

Parameter	Symbol	Value	Unit
Drain-Source Voltage	VDS	-60	V
Gate-Source Voltage	VGS	±20	
Continuous Drain Current	ID	-8.8	A
Pulsed Diode Curren	IDM	-35	
Linear Derating Factor		0.33	W/°C
Linear Derating Factor (PCB Mount)		0.02	W/°C
Power Dissipation	PD	50	W
Thermal Resistance from Junction to Ambient (t≤10s)	RθJA	45	°C/W
Single Pulse Avalanche Energy	EAS	300	mJ
Repetitive Avalanche Current	I AR	-8.8	A
Repetitive Avalanche Energy	EAR	5.0	mJ
Peak Diode Recovery dV/dt	dV/dt	-4.5	V/ns
Maximum Junction-to-Ambient	RthJA	110	°C/W
Operating Junction	TJ	150	°C
Storage Temperature	TSTG	-55~+155	

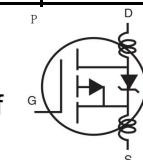
Notes :

- 1.Repetitive rating; pulse width limited by maximum junction temperature
- 2.VDD = 25 V, starting TJ = 25 °C, L = 4.5 μH, RG = 25 Ω, IAS = -8.8 A
- 3.ISD ≤ -11 A, dI/dt ≤ 140 A/μs, VDD ≤ VDS, '
- 4.1.6 mm from case.
- 5.When mounted on 1" square PCB (FR-4 or G-10 material).

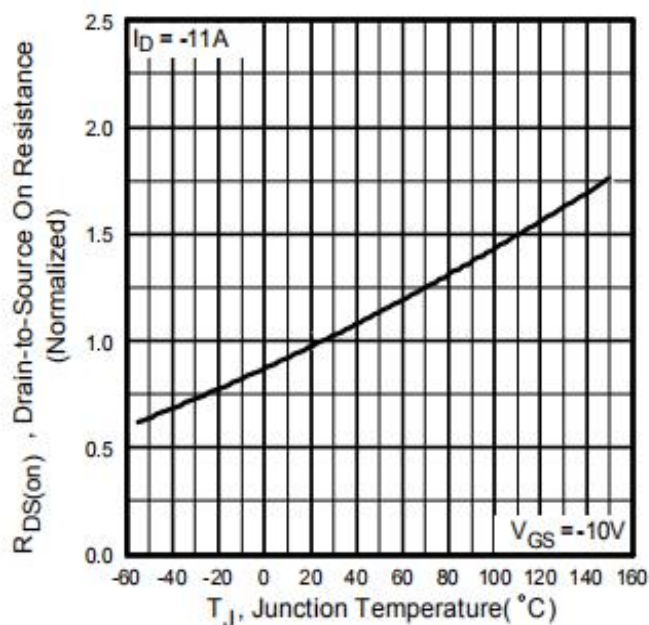
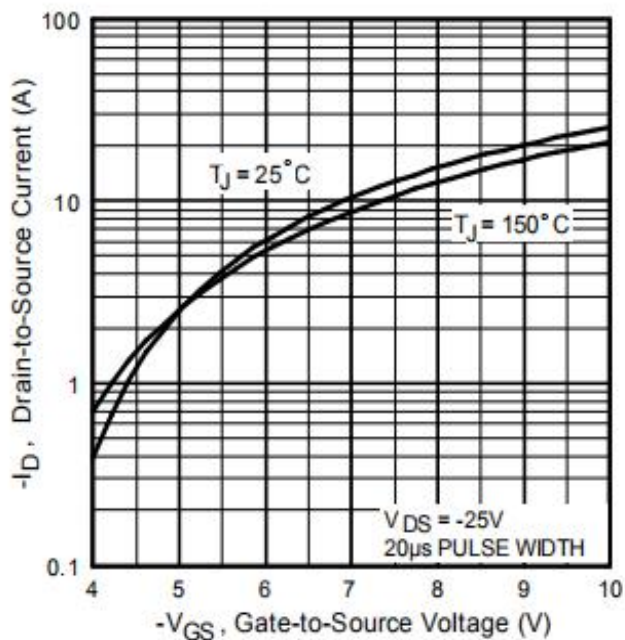
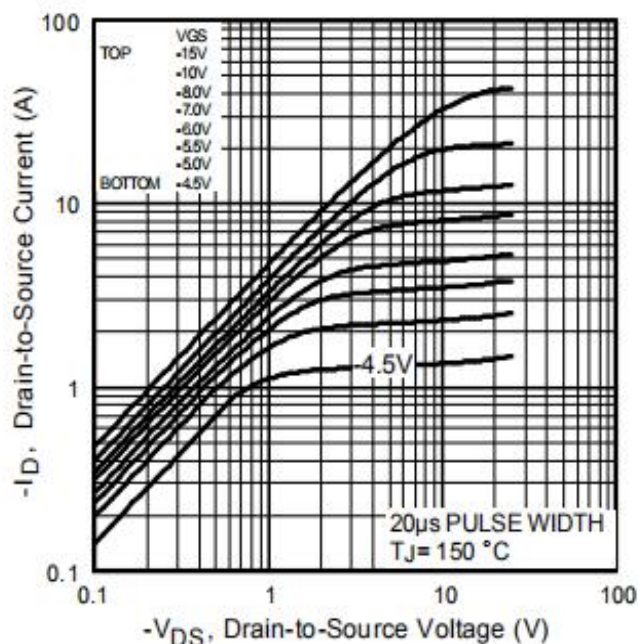
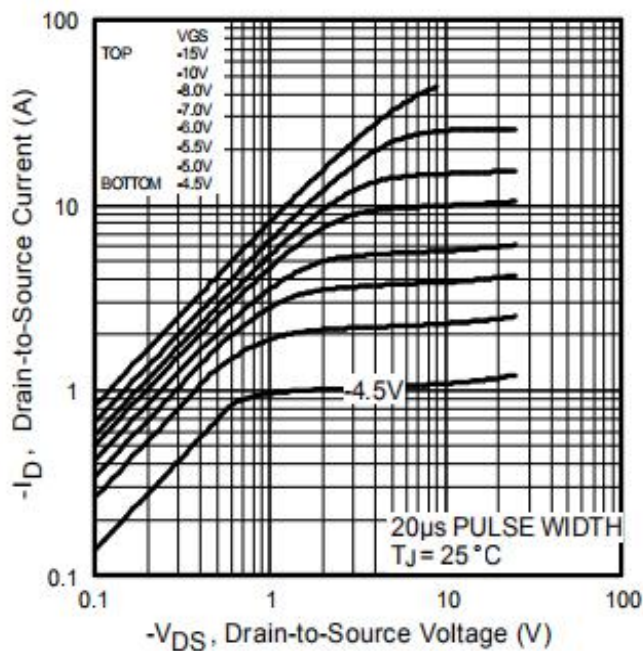
MOSFET ELECTRICAL CHARACTERISTICS

Static Electrical Characteristics (Ta = 25 °C Unless Otherwise Noted)

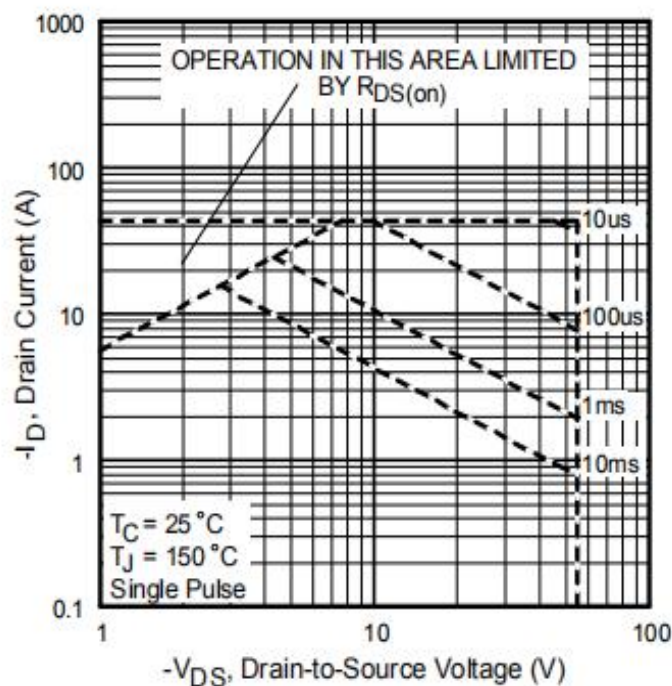
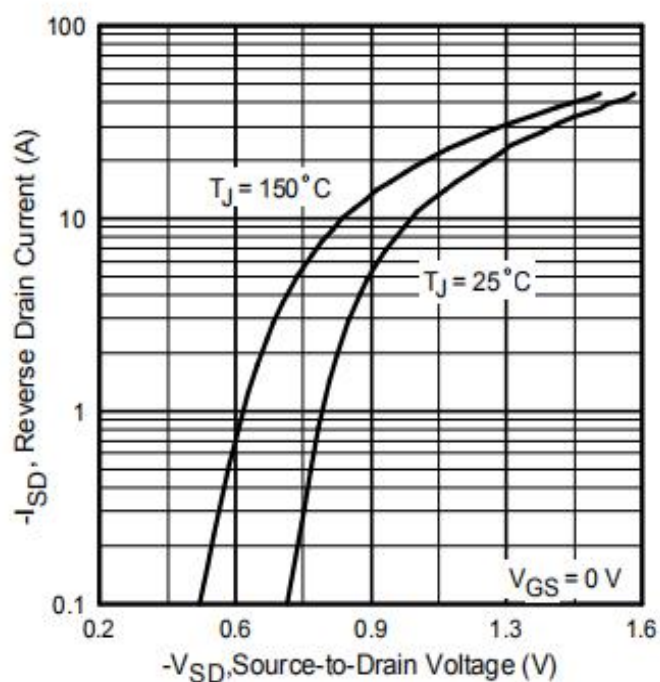
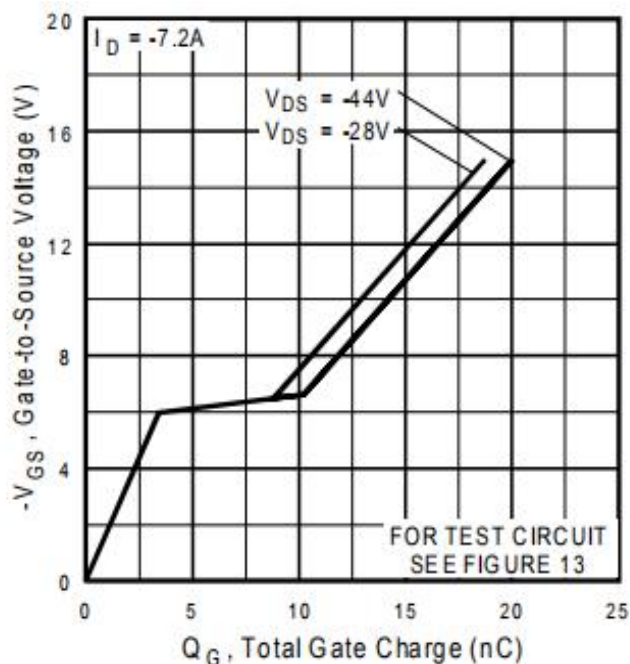
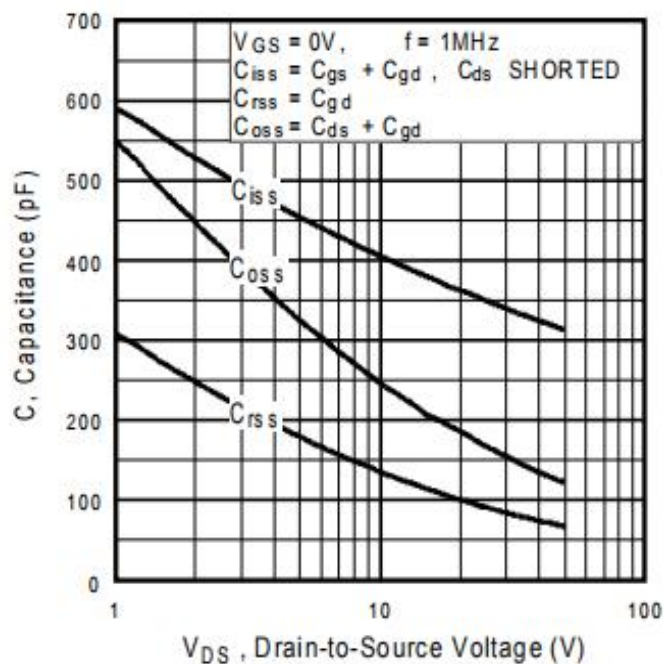
Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Static						
Drain-source breakdown voltage	V(BR)DSS	VGS = 0V, ID = - 250μA	-60			V
Gate-source threshold voltage	VGS(th)	VDS = VGS, ID = -250μA	-2		-4	V
Gate-source leakage	IGSS	VDS = 0V, VGS = ±20V			±100	nA
Zero gate voltage drain current	IDSS	VDS = -60V, VGS = 0V			-100	μA
Drain-source on-state resistancea	RDS(on)	VGS = -10V, ID = -5.3A		75	200	mΩ
Forward transconductancea	gfs	VDS = -25V, ID = -5.3A	2.9			S
Diode forward voltage	VSD	IS = -7.2A, VGS = 0V			-1.8	V
Dynamic						
Input capacitance	Ciss	VDS = -25V, VGS = 0V, f = 1MHz		570		pF
Output capacitance	Coss			360		pF
Reverse transfer capacitanceb	Crss			65		pF
Total gate charge	Qg	VDS = -48V, VGS = - 10V, ID = -11A			19	nC
Gate-source charge	Qgs				5.4	nC
Gate-drain charge	Qgd				11	nC
Gate resistance	Rg	f = 1MHz				Ω
Switchingb						
Turn-on delay time	td(on)	VDD = -30V RD = 3Ω, ID = -11A, VGEN = -10V, Rg = 18Ω		13		ns
Rise time	tr			68		ns
Turn-off delay time	td(off)			15		ns
Fall time	tf			29		ns
Internal Drain Inductance	LD	Between lead, 6 mm (0.25") from package and center of die contact		4.5		nH
Internal Source Inductance	LS			7.5		nH
Drain-Source Diode Characteristics						
Reverse Recovery Time	trr	IF = -11A, dI/dt = 100A/s		100	200	ns
Reverse Recovery Charge	Qrr	IF = -11A, dI/dt = 100A/s		0.32	0.64	μC
Continuous Source-Drain Diode Current	IS	MOSFET symbol showing the integral reverse p - n junction diode			-8.8	A
Pulsed Diode Forward Current	ISM				-35	A



TYPICAL CHARACTERISTICS :



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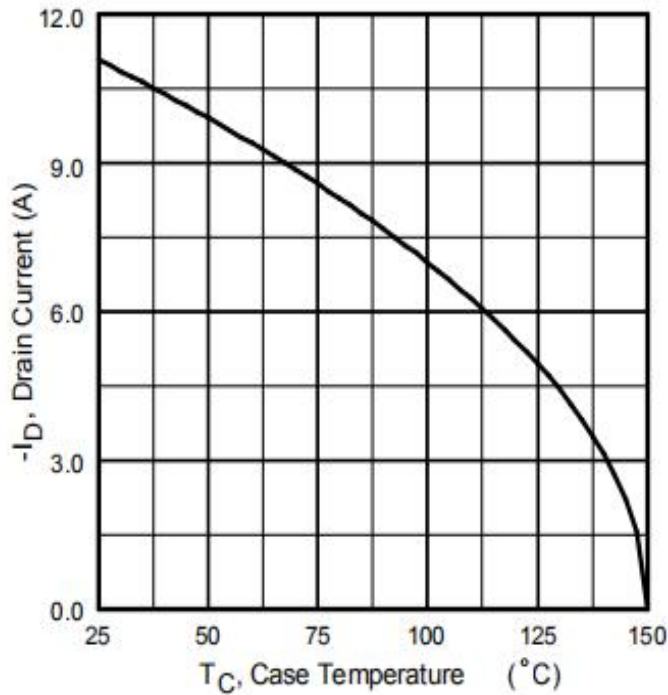


Fig 9. Maximum Drain Current Vs. Case Temperature

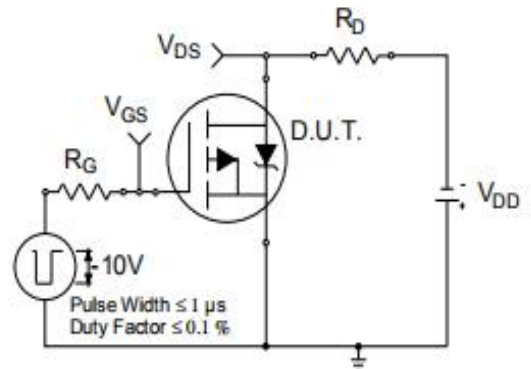


Fig 10a. Switching Time Test Circuit

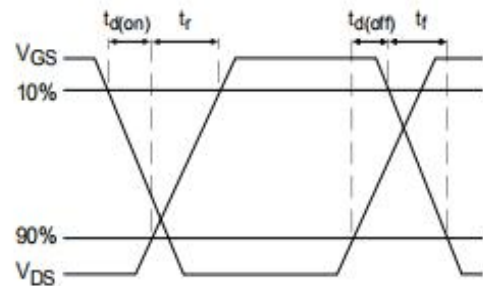


Fig 10b. Switching Time Waveforms

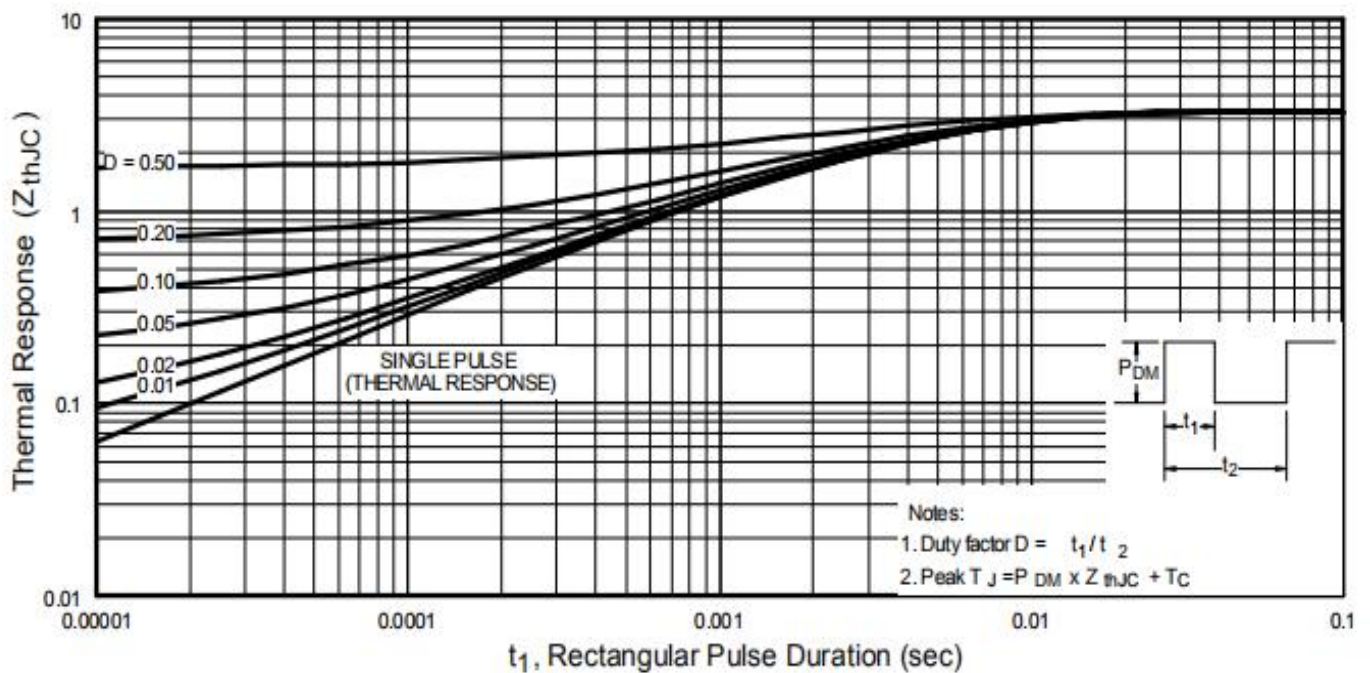


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case

TYPICAL CHARACTERISTICS :

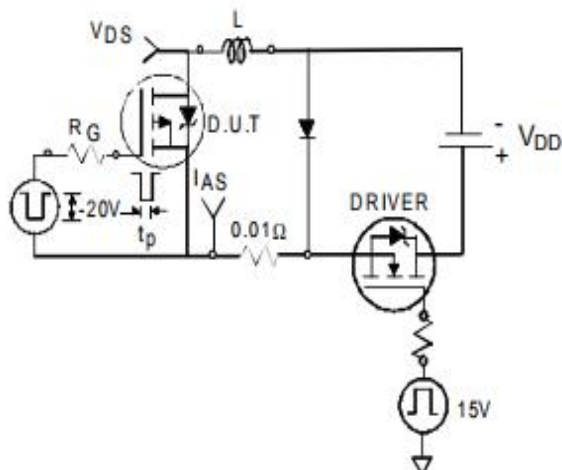


Fig 12a. Unclamped Inductive Test Circuit

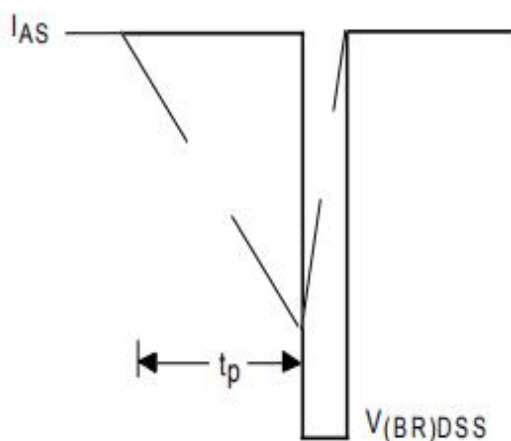


Fig 12b. Unclamped Inductive Waveforms

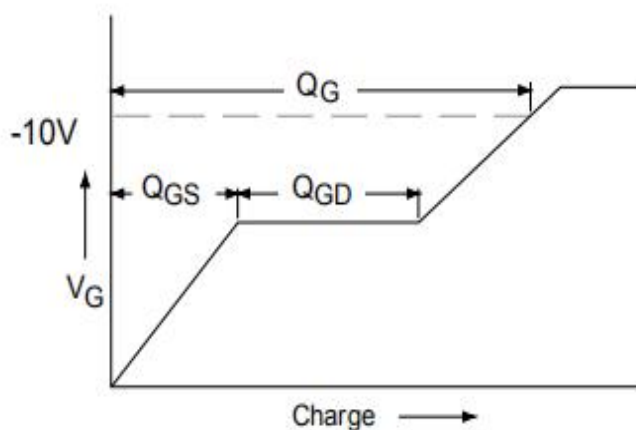


Fig 13a. Basic Gate Charge Waveform

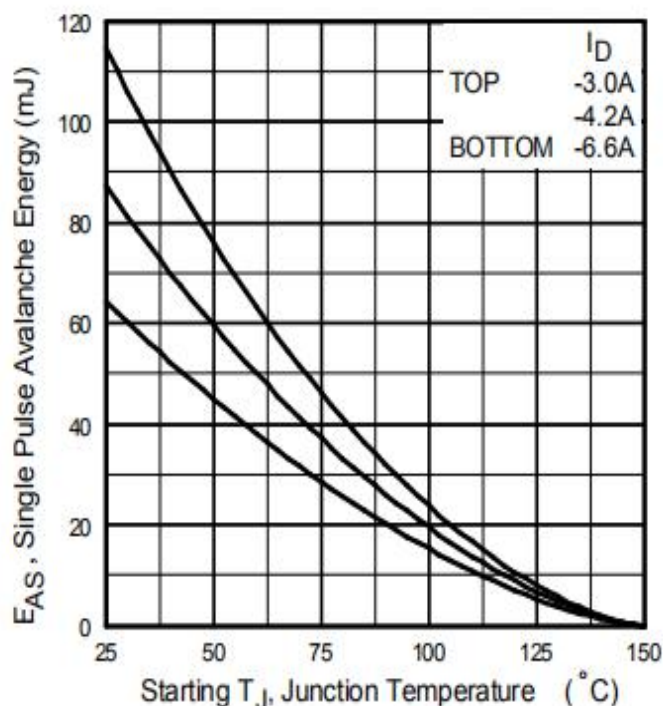


Fig 12c. Maximum Avalanche Energy Vs. Drain Current

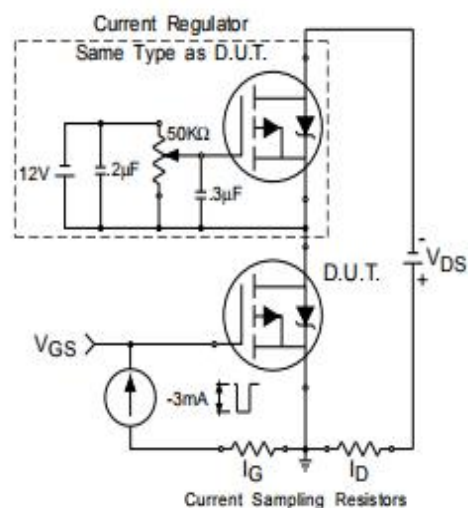
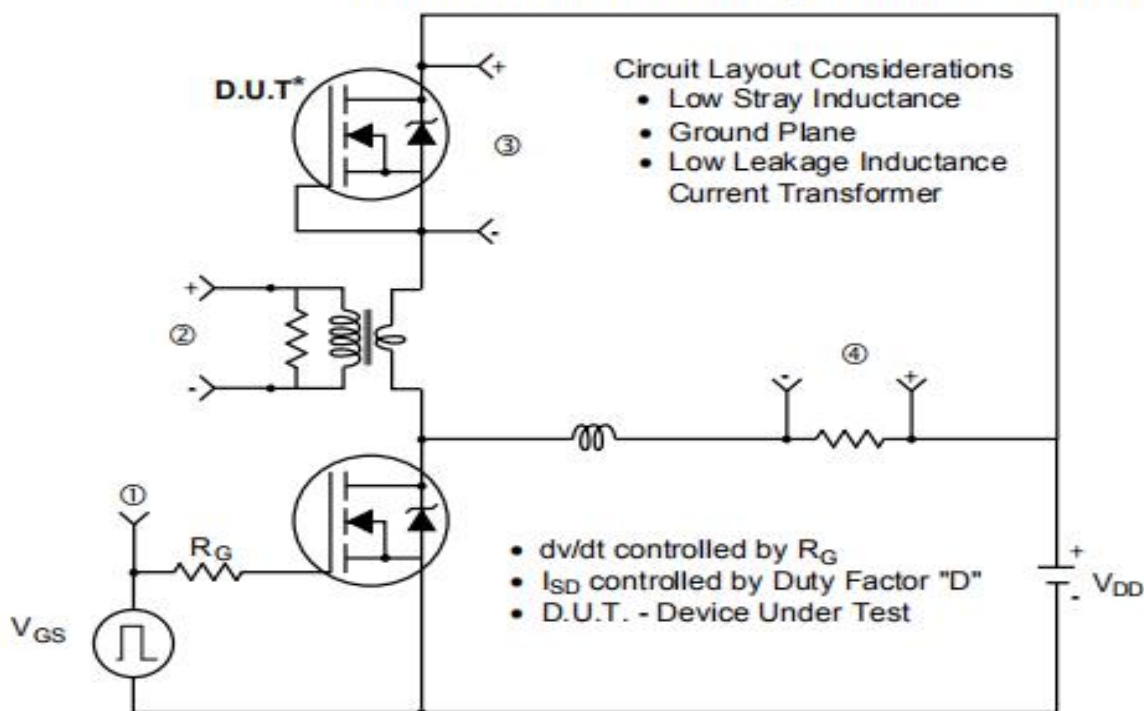


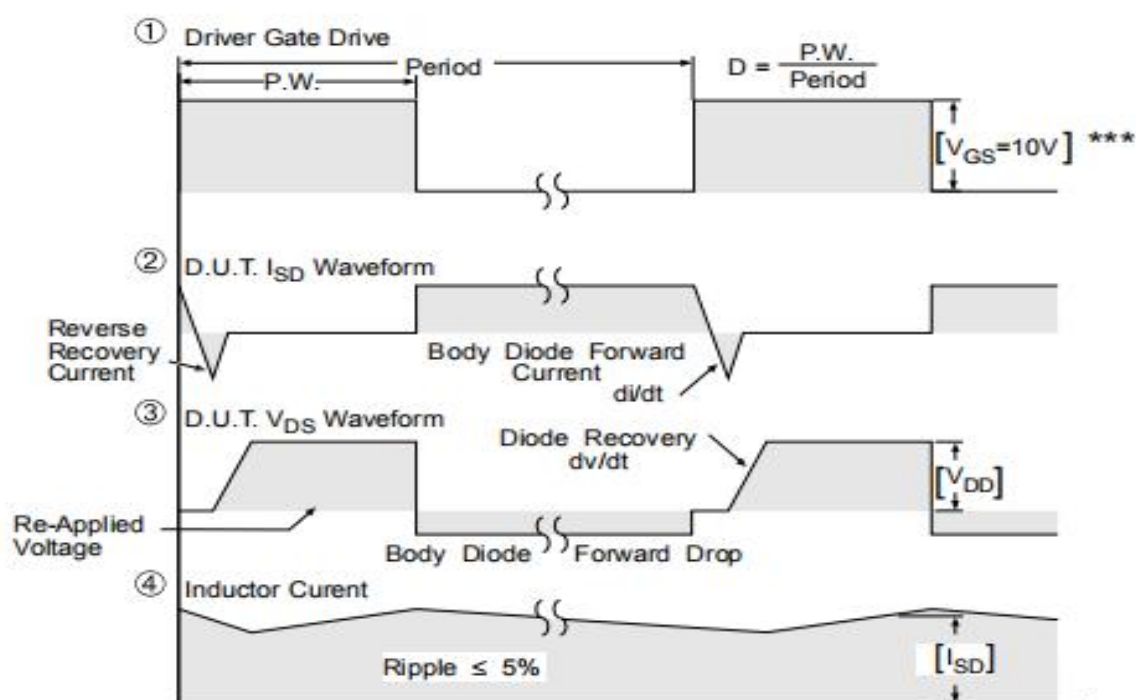
Fig 13b. Gate Charge Test Circuit

TYPICAL CHARACTERISTICS :

Peak Diode Recovery dv/dt Test Circuit

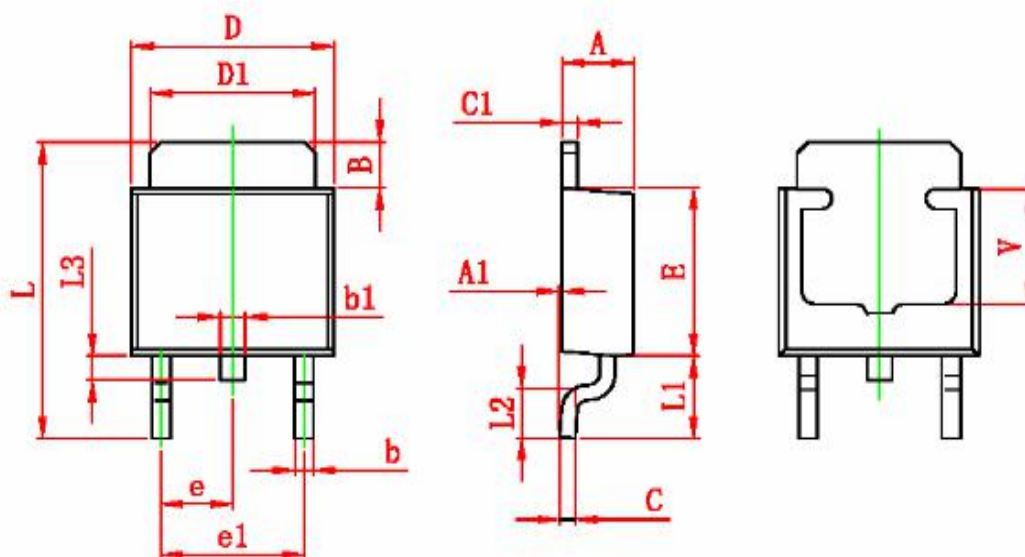


* Reverse Polarity of D.U.T for P-Channel



*** $V_{GS} = 5.0V$ for Logic Level and 3V Drive Devices

Fig 14. For P-Channel HEXFETS

PACKAGE OUTLINE DIMENSIONS :


Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	2.200	2.400	0.087	0.094
A1	0.000	0.127	0.000	0.005
B	1.350	1.650	0.053	0.065
b	0.500	0.700	0.020	0.028
b1	0.700	0.900	0.028	0.035
c	0.430	0.580	0.017	0.023
c1	0.430	0.580	0.017	0.023
D	6.350	6.650	0.250	0.262
D1	5.200	5.400	0.205	0.213
E	5.400	5.700	0.213	0.224
e	2.300 TYP		0.091 TYP	
e1	4.500	4.700	0.177	0.185
L	9.500	9.900	0.374	0.390
L1	2.550	2.900	0.100	0.114
L2	1.400	1.780	0.055	0.070
L3	0.350	0.650	0.014	0.026
V	3.80 REF		0.150 REF	